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Advantages of Isotropic PCB Routing

This article discusses whether arbitrary-direction routing and rounded, dog-leg-free wires are a whim of the TopoR CAD developers or a technically justified solution.

1. Origins of the orthogonal routing habit

It is well known that all new things have a hard time breaking through. At the same time, as the saying goes, all new things are long forgotten old things.

More than 40 years have passed since the publication of the "wave" algorithm - i. e. the Lee algorithm -for solving maze routing problems. The earliest grid autorouters also appeared about 40 years ago. Before the introduction of automated design systems, printed circuit topology was designed manually. It was quite natural that nobody drew polylines instead of straight lines; moreover, the angles of wires were usually rounded. The look of the first PCBs designed by automated systems caused discontent, perplexity, and rejection. However, as time passed, CAD systems became more and more sophisticated and efficient. Gradually designers got used to the wires shape and accepted the situation, especially so because automation had considerably increased their productivity. After forty years, a whole generation of specialists changed, and now there a very few people left who can still remember manual design. These days the non-orthogonal layout, rounded wires are perceived by many as something absurd, irregular, and unconventional.

One of the most frequently used arguments is, "Orthogonal topology looks good, and arbitrary-angle topology does not."

The figure below shows a fragment of a PCB routed by one of the popular autorouters. One can see numerous bent wires; this is easy to explain (such are the algorithms), but not to justify. The second figure shows a fragment of a board routed by the TopoR topological router… [1]

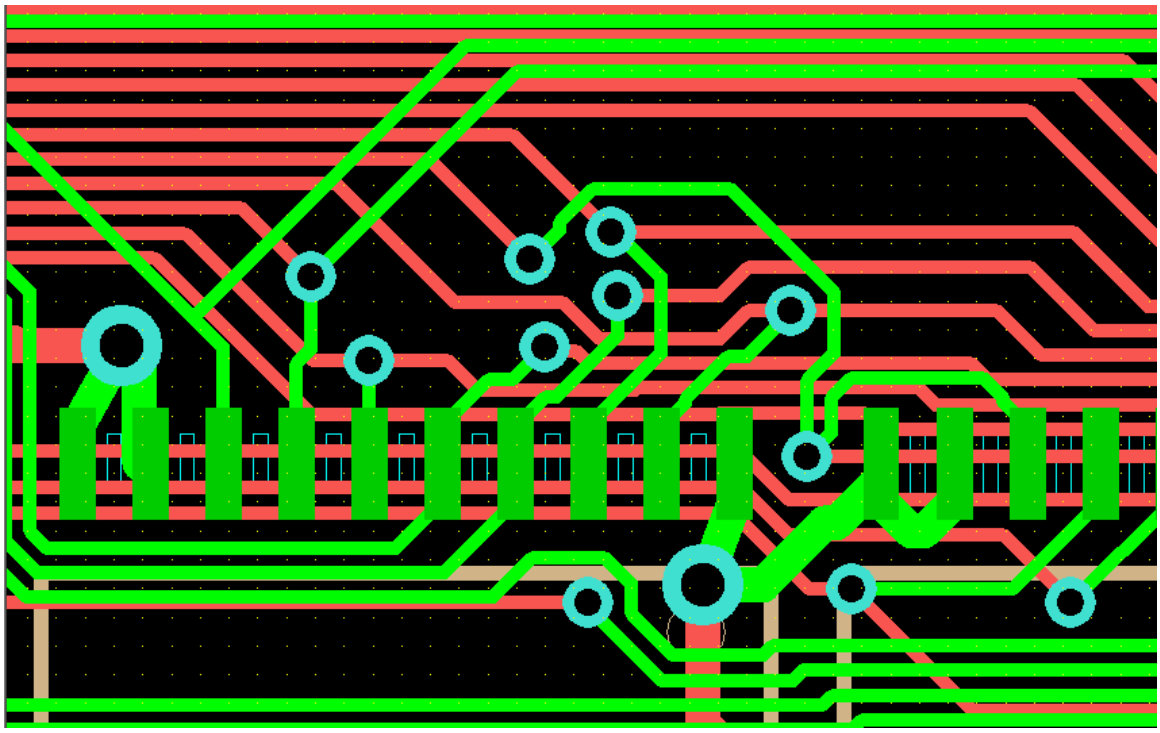

Figure 1. Fragment of a PCB routed by a conventional autorouter.

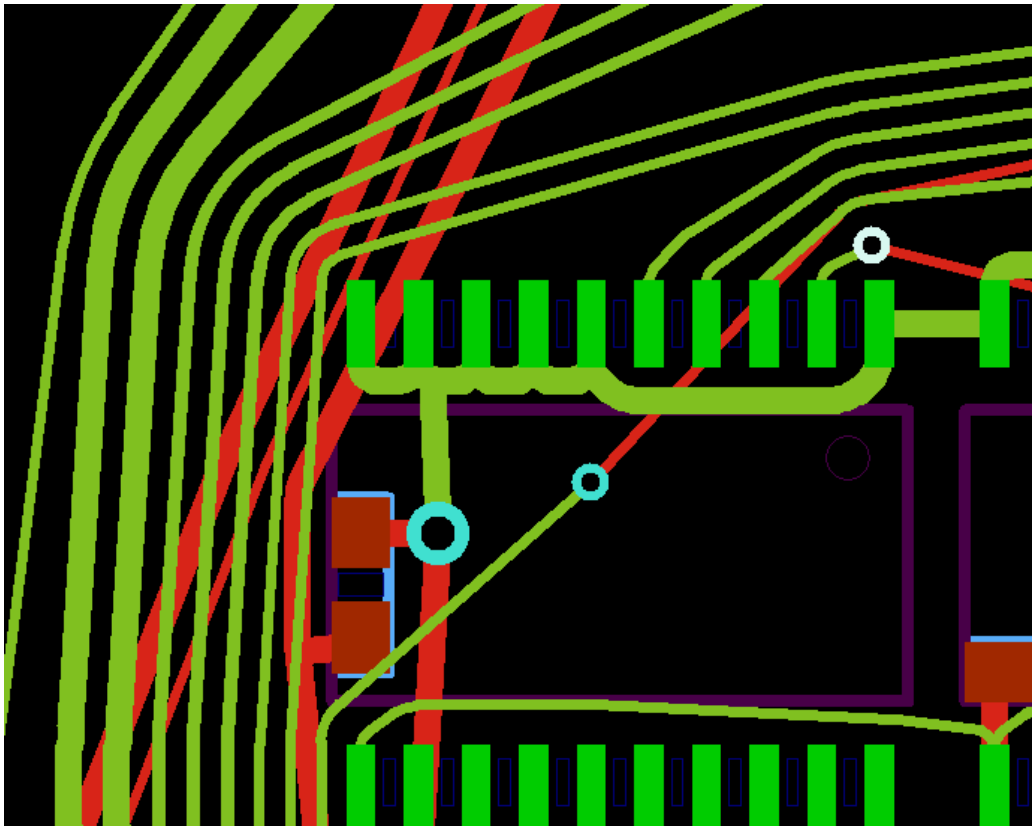

Figure 2. Fragment of a PCB routed by the TopoR router.

As regards aesthetics, tastes differ, so let’s consider the technical side.

Authors' stories about their creation usually sound less than convincing to others, so when speaking about the advantages of topological routing, let's refer to the publications of competent specialists.

Routing is searching for a compromise solution for laying out multiple routes while meeting a number of conflicting criteria (total wires length, number of vias) and observing of different design and technological constraints, which are primarily metrical. Usually, due to the complexity of the task, no attempt is made to achieve a topology that would be optimal in any sense. The stated purpose is to achieve the maximum rate of complete routes.

In most printed circuit CAD systems the task of routing interconnections is defined as iterative search for paths between pairs of points in a maze formed by contact pads, keepouts, and previously routed wires. The laid-out path is locked and becomes part of the maze.

As a result of limited throughput capacity of the printed circuit areas, the routes are often excessively long, and therefore, the number of vias increases. Having to go around the stationary component increases the length of the route and creates obstacles for laying out other routes.

All other tasks (minimization of the total wire length and the number of vias, moving the wires apart locally to reduce spurious coupling, etc.) are usually done after the main result is achieved. These improvements are made to the single topology variant that has been obtained. Of course, refinement possibilities presented by such localized procedures are quite modest. In most cases the primary criterion for assessing the routing quality is whether the circuit works at all.

Meanwhile, the important topology quality indicators that are overlooked include workability and reliability, which depend in part on the number of bottlenecks with minimal clearance and their length, on the length of parallel paths on each layer, and conductor overlap area on adjacent layers.

2. PCB Space Utilization

Popular printed circuit topology design systems route the wires along paths that are vertical, horizontal or slanted at 45°.

Figure 3 from the article devoted to the TRL single-layer autorouting system demonstrates the advantages of any-angle routing. One can see that only the rightmost variant allows laying out four routes instead of three in the gap between the rectangular regions; i. e. PCB space is used more efficiently.

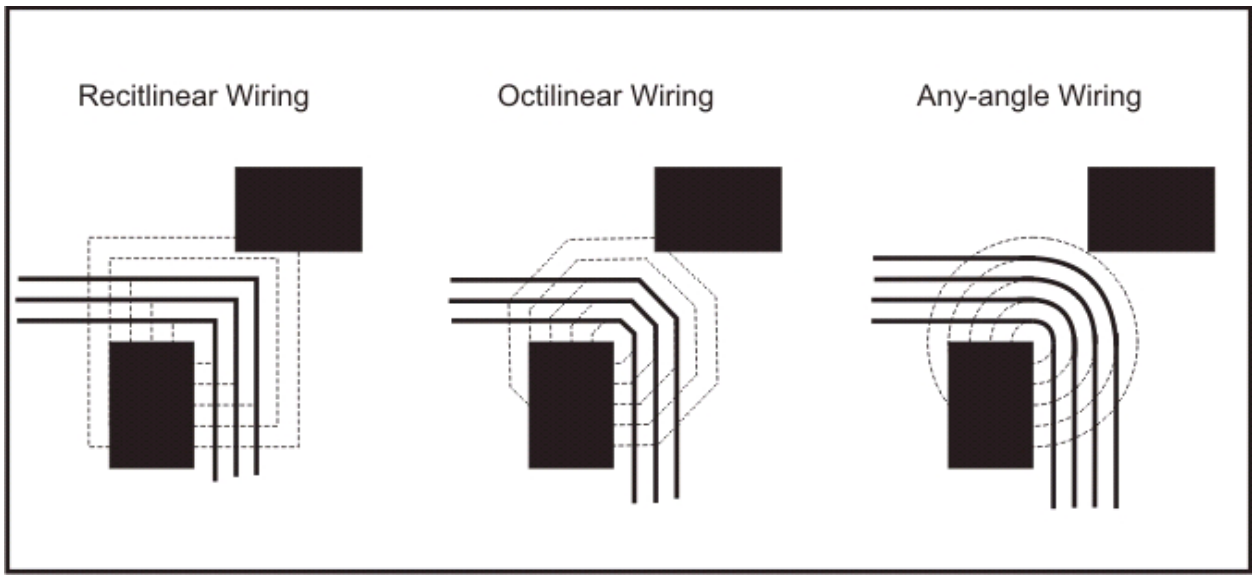

Figure 3. PCB space usage for three methods of routing.

The next figure shows a sample case where the required clearance can be provided only by smoothed wires. The wires pass from one circular arc to another; the required clearance is maintained along the whole length. Any diversion from the circular arc path will lead to clearance violation. Therefore, any-angle routing with smoothed wires provides more efficient PCB space utilization; the area of a circle is always less than the area of a circumscribed polygon.

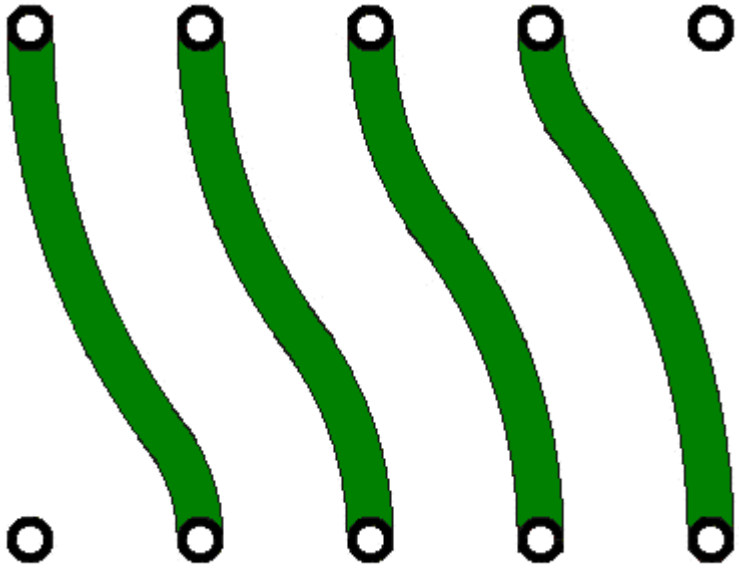

Figure 4. The only possible variant with minimal wire length and uniform clearance.

3. Smooth, Non-Bent Wires

The conducting pattern defines to a large extent the workability and manufacturing reliability of PCBs.

When routing wires, one should avoid sharp corners. Inside such a corner a kind of pocket is formed with poorly etched areas, where solder buildups and spikes are formed during soldering. Due to a slight compression stress in galvanic deposits induced by soldering temperature, a sharp corner may peel off the base. If a wire has high electric potential, the corner apex gains high electric-field gradient; contaminations are accumulated at this point due to electrostatic deposition of dust. This creates an electric breakdown hazard. [2]

At the place where a conductor makes a 90-degree turn, signal bouncing may occur. This happens mainly due to the change of wire width. At the corner the route width is increased 1.414 times, which results in transfer line parameter discrepancy, and especially to distributed capacitance and self-inductance of the line. [4]

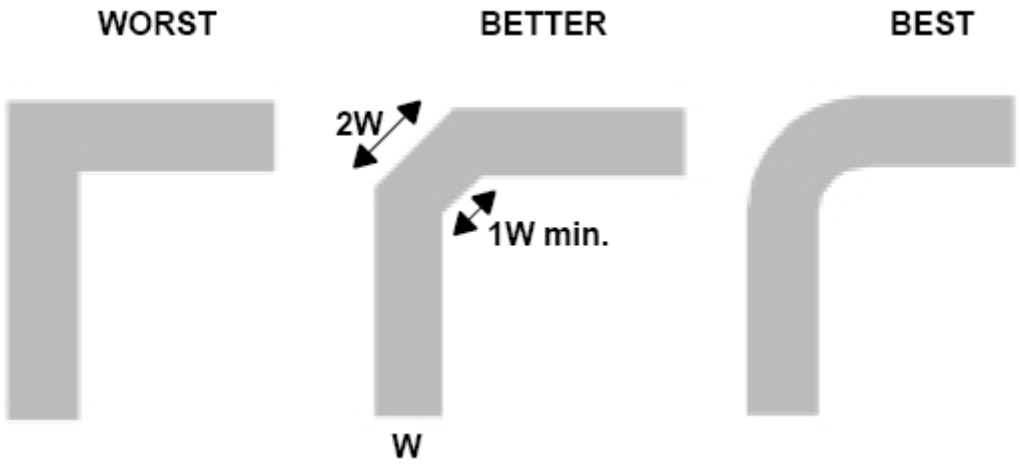

Figure 5. Smoothing the corners of wires.

One of the distinctions of the topology created by the TopoR system is smooth, dog-leg-free wires, and therefore absence of problems described above.

4. Predominant Layer Routing Directions

“One should keep in mind that when the PCB is heated during heat treatment, thermal reflow, drying, soldering, etc., the balance of patterns on the two sides of the board substantially affects its deformation ratio due to the

difference in mechanical stress. *The widely used rule of opposite sides' pattern orthogonality leads to twisting of a PCB*." [2]

It should be noted that the cause of the twisting is not pattern orthogonality itself, but the global directional uniformity of the conductors on the layer. In the topology created by TopoR the wires in adjacent layers are roughly orthogonal, but in different areas of the board the directions vary, that is why layer anisotropy is not a global effect.

5. Electromagnetic Interference Level

Wires located opposite one another on adjacent layers form a long film capacitor. If two conductors are close to each other, then capacitive and inductive coupling occurs between them (Figure 6).

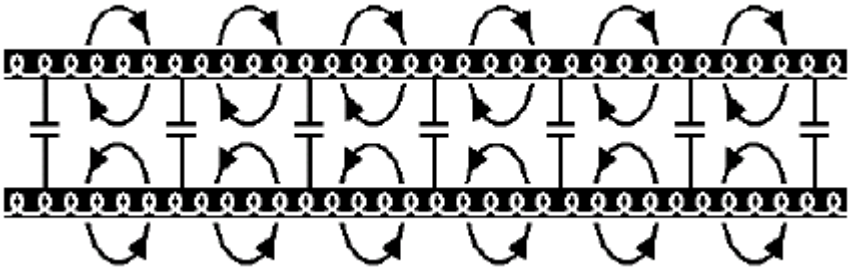

Figure 6. Interference between two parallel signal wires.

It is necessary to remember, that every new via, i. e. interlayer connection, adds spurious inductance. For example, if the opening has a diameter of 0.4mm and is 1.5mm high, which are quite frequently-used values, then its inductance is 1.1nH. [4]

The TopoR CAD system almost never creates long wire segments laid out parallel to each other in adjacent layers. The option to specify the minimal and nominal clearance between wires significantly reduces the number and length of bottlenecks on a single layer. The number of vias in the topology produced by TopoR is usually many times less compared to the topology created with any other system.

Besides, all aforementioned factors along with reduction of total wire length and absence of predominant routing directions help decrease the electromagnetic interference level.

We would like to dispel one widespread delusion. When looking at wires smoothly going around obstacles, developers often note that a straight wire has much less inductance than an arced one, making the conclusion that the topology created with the TopoR CAD system has greater overall inductance.

In reality, most CAD systems perform routing with a predominant direction on each layer; therefore, wire direction rarely changes on a single layer.

In order to estimate the wire inductance, it is not the individual layer topology that should be considered, but the combined topology. This will show clearly not only wire bending, but even loops.

Loop inductance depends on the loop area, and it does not matter whether it is rectangular or circular. The surface area of a wire laid out by TopoR is usually considerably less than in other CAD systems. It should be noted that rounding of prominent corners reduces the area of a convex geometric shape.

6. Complexity and Cost of Manufacturing

One of the factors affecting the printed circuit board manufacturing cost is the number of vias per square decimeter. On average, the estimated cost of vias is $1 per additional 300 (exceeding 250) vias per square decimeter.

The durability of a hard-alloy drill is about 1000 openings. The average price of one drill from 0.3 to 3.0 mm in diameter is about $2.

An excessive number of openings increases manufacturing cost and drilling time; every 1000 openings take an extra 2.5-3 minutes of drilling for each board. This results in considerable material and time expenses for large-scale and mass production.

During development of multilayer printed circuit boards, one of the aims to achieve is minimizing the number of layers, because each extra layer significantly increases the PCB cost. For boards employed in high-performance and high-frequency systems, increasing the number of signal layers requires twice as many layers to maintain the transmission line characteristics—signal layers must be padded with ground and power layers to provide shielding in such devices. [2]

In boards with BGA components the number of layers often depends mainly on the number of pad rows of such components and on established technological constraints, such as the minimum wire width and minimum clearance. In a number of CAD systems BGA component internal space routing is performed according to a template, because the main purpose is to avoid blocking pads and to lead all routes to the component’s outer edges. But prescribing the mandatory routing directions results in layout deterioration and does not consider the fact that if a microchip has equipotential and non-connected pads, then in some cases the number of layers needed to provide connections can be reduced.

Compared to other systems, CAD TopoR helps reduce the total wire length by 25-40% and to make the number of vias 2-3 times less. This means that more free space becomes available on the board; it is possible either to increase wire clearance and contact pad size, or to reduce the board size or the number of layers.

Isotropic routing used in the TopoR CAD system allows you to considerably speed up board development, to increase board workability, reliability and quality,

to lower the electromagnetic interference level, and to reduce manufacturing costs. Thereby, isotropic routing is not a whim of TopoR developers, but a technically justified solution.

Bibliography:

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